Abstract of the Disclosure

An adjustable timing circuit includes non-volatile programmable fuses and adjustable delay elements. A propagation time of the delay element is selected with the non-volatile fuses. The delay element can include capacitors that are selectively coupled to a propagation path in response to the data stored in the fuse circuits. In one embodiment, data stored in the programmed fuses is copied to volatile latch circuits for use during operation of the timing circuit. The adjustable timing circuit can be provided in any integrated circuit, but is particularly useful in memory devices. The timing system allows for testing and fine-tuning signal processing in the integrated circuits.